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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,497	12/19/2001	William G. En	50432-477	1401

7590 11/20/2002
McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

SOWARD, IDA M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/021,497

Applicant(s)

EN ET AL.

Examiner

Ida M Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 11-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 4-22-02 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed October 31, 2002.

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-10 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that the Examiner has not shown that the device of the Group I invention could be made by a process materially different from those/that of the Group II invention. This is not found persuasive because the wafer as claimed could have been made by another and materially different manufacturing method such as removing portions of the conductive layer by a sputter etch or plasma etch.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character

"50" has been used to designate both **gate electrode** and **wafer**;

"54" has been used to designate both **interconnect layer** and **shallow trench isolation regions**;

"56" has been used to designate both **sidewall spacers** and **gate oxide layer**;
and

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"58" has been used to designate both **channel region** and **nitride stack layer**.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **58** in Figure 7. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 7 in view of Tuan et al. (US 2002/0151141 A1) and Hobbs et al. (US 6,171,910 B1).

Admitted Prior Art Figure 7 teaches a wafer comprising: a base layer **42**; an active region in the base; a gate dielectric layer **46** formed on the active region; a conductive layer **50** formed on the gate dielectric layer; a plurality of shallow trench

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isolation regions **44** formed in the wafer; and a metal interconnect layer **54** formed over the conductive layer. However, Admitted Prior Art Figure 7 fails to teach a wafer being divided into a plurality of first, second and third portions. Tuan et al. teach a wafer being divided into a plurality of first, second and third portions; the first portion comprise gate dielectric capacitor (a transistor), the gate dielectric capacitors comprise a first electrode layer **124**, an insulating layer **108**, and a second electrode layer **128** made of polysilicon contacting an isolation region **1010**; wherein the first electrode layer is formed from the active layer, the insulating layer is formed from the gate dielectric layer, and the second electrode is formed from the conductive layer; and the third portions (containing no active layer) comprise second dummy structures **141**, the second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region **1010** and the second electrode layer of the second dummy structures if formed from the conductive layer (Figure 3, page 3, paragraphs [0034]-[0042]). Hobbs et al. teach the second portions comprise first dummy structures **201 & 202**, the first dummy structures comprise a first electrode layer **84** and an insulating layer **82**; wherein the first electrode layer of the first dummy structures is formed from the doped silicon active layer **32** and the insulating layer of the first dummy structures is formed from the gate dielectric layer (Figure 5, col. 4, lines 22-40) and not containing a conductive layer in **66** (Figure 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the gate dielectric structure of Admitted Prior Art Figure 7 with the

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first, second and third portions of Tuan et al. and the dummy structures of Hobbs et al. to reduce tunneling leakage.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to dummy structure devices:

Bertin et al. (US 6,396,121 B1)

Bertin et al. (US 2002/0105051 A1)

Janai et al. (5,679,967)

Takasugi (4,975,382).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

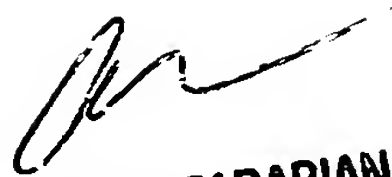
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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November 18, 2002



AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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